Rambus

Advanced Memory Interfaces for High-Performance Systems

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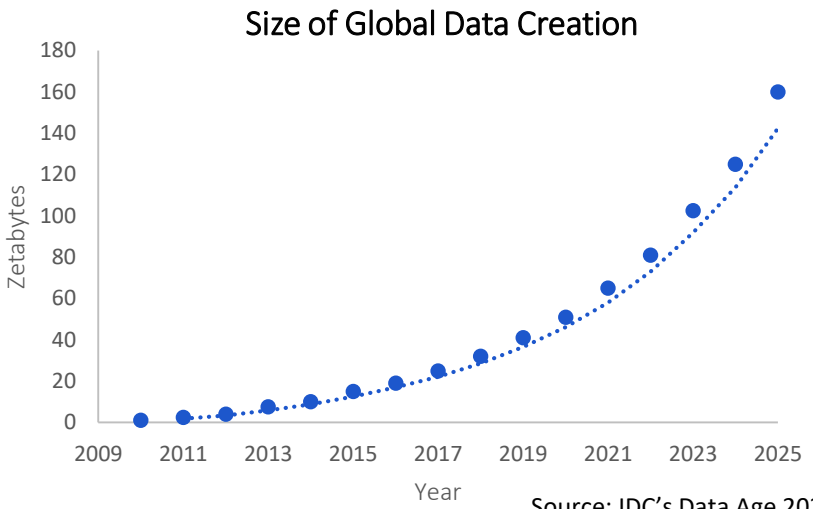
DAC June 4, 2019

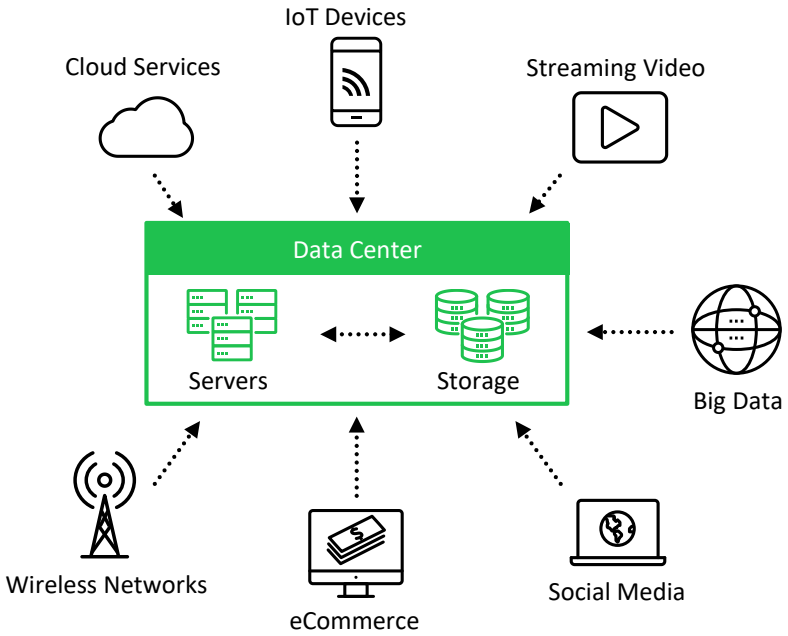
Exponential Data Growth Mandates Increased Bandwidth

Exponential data growth is driving performance requirements and new architectures



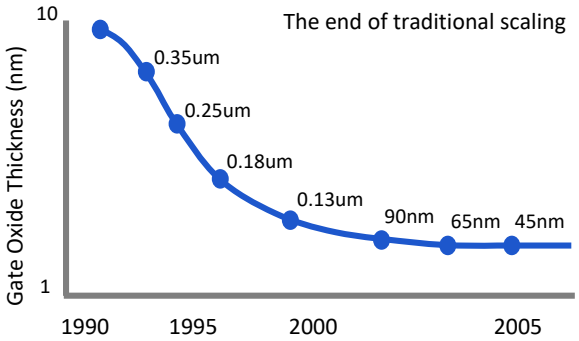
Source: IDC's Data Age 2025 Study

High-speed interconnects and Memory bandwidth are key to data center performance and growth



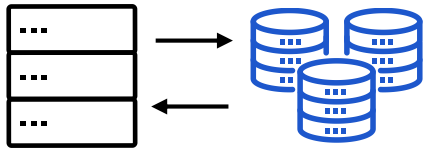
Improvement Needed in Memory Systems

Limits of DRAM Scaling



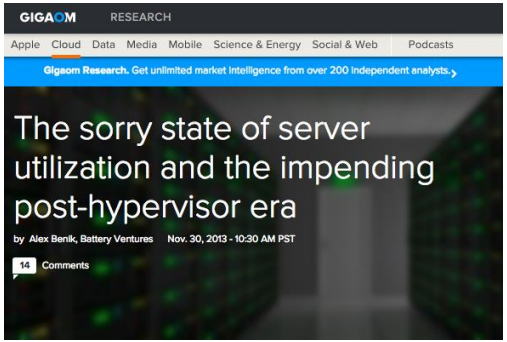
Cost per bit of DRAM no longer scaling with process

Big Data Analytics



Massive and growing data sets are straining data center architecture

Low CPU Utilization

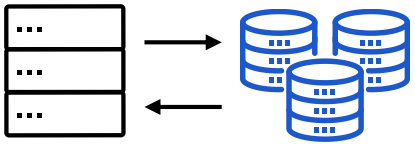


Number of CPU cores scaling *faster than memory can support*

These challenges are opportunities for Innovation at the System and Semiconductor level

Challenges for Servers and Data Centers

Performance, power efficiency, and TCO are increasingly limited by data movement



Large volumes of data being moved to computing resources, reducing performance, increasing power consumption, and increasing TCO

Expanding Memory Near Processing:

Move data closer to the processing

Near-Data Processing:

Move processing closer to the data

Emerging Applications: Driving Compute/Memory Evolution

Memory Bandwidth is a Critical Bottleneck!

Applications

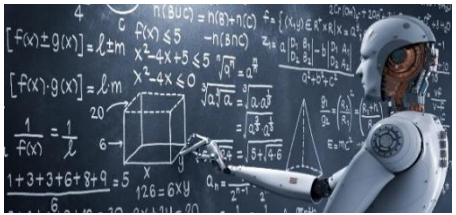
- **Networking:** Wireline and Next Generation Wireless Infrastructure
- **Automotive:** ADAS and full autonomous
- **AI: Machine Learning and Deep Learning:** Advanced neural networks

Custom silicon and new system architectures

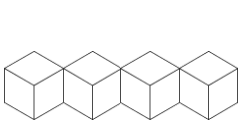
- Emerging applications reaching the limits of current hardware architectures
- Increasing reliance on accelerators and specialized silicon such as neural networks
- Memory IP is critical for addressing a key bottleneck in these systems

Advanced Driver Assistance Systems

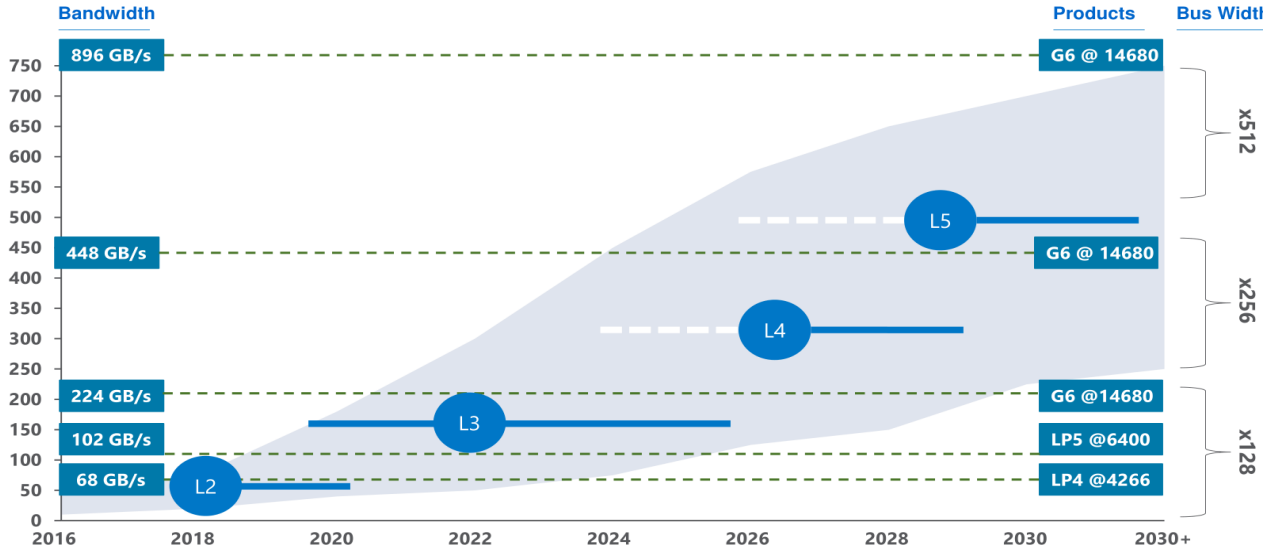
Machine Learning / Neural Networks



Blockchain / Cryptocurrency Mining



Emerging Applications: Automotive



Source : https://www.anandtech.com/show/12362/micron-rambus-others-team-up-to-spur-gddr6-adoption

- Complex data processing requires large and fast memory – Sense, Perceive, and take action
- Automated Driver Assisted Systems (ADAS) need bandwidth >>300GBps

Major Applications and Key Memory System Challenges

Hyperscale Computing, Consumer Devices

Today: DDR4 (3.2Gbps)
Future: DDR5 (6.4Gbps)

Key challenges:
- Multi-drop topology
- Capacity
- Power-efficiency
- Bandwidth

Graphics, Gaming, AI, HPC

Today: HBM2 (2Gbps),
GDDR6 (16Gbps)
Future: > 2Gbps (HBM),
> 16Gbps (GDDR)

Key challenges:
- Signal integrity
- Cost
- Power-efficiency
- System engineering

Networking

Today: DDR4 (3.2Gbps)
Future: > 2Gbps (HBM),
> 16Gbps (GDDR)

Key challenges:
- Bandwidth
- Power-efficiency
- Form factor

Phones, Tablets, Mobile Devices

Today: LPDDR4 (4.266Gbps)
Future: LPDDR5 (6.4Gbps)

Key challenges:
- Power-efficiency
- Bandwidth
- System engineering

Memory Comparison

Parameter	GDDR6	HBM2	DDR4	LPDDR4X
Bandwidth (Gbps)	High (512)	Highest (2000)	Medium (200)	Low-Medium (136)
Data Rate (Gbps)	16	2	3.2	4.266
Interface width (bits)	32	1024	64	32
Board Area / System Design	Medium / Medium	Small / Complex	Large / Easy	Large / Medium
Efficiency (mW/Gbps)	Moderate (10)	Highest (2)	Moderate (10)	High (3)
Cost ($)	Medium	High	Low	Medium
Reliability/Yield	Good	Moderate	Good	Good

Rambus Memory IP Solutions

Memory PHY Solutions for Networking, AI, Data Center and Automotive

DDR4/3

- 3200Mbps
- x16 – x72-bits
- 1-4 Ranks
- DFI 4.0

Si

HBM2/E

- 2000 - 3200Mbps
- 1024-bit
- 2.5D design architecture

Si

GDDR6

- 12 - 16Gbps
- 2 x 16-bit channels
- Validated with Memory Controller

IN LAB

DDR5 &HBM3

- DDR5: 4.8 – 6.4Gbps
- HBM3: 4Gbps

IN DEVELOPMENT/ ROADMAP

Integrated tools for easy bring-up and characterization

LabStation Platform

- Easy-to-use PC Interface
- Interface to 3rd party software
- Pre-defined test scripts
- PHY control settings
- External instrument control
- System characteristics and analysis

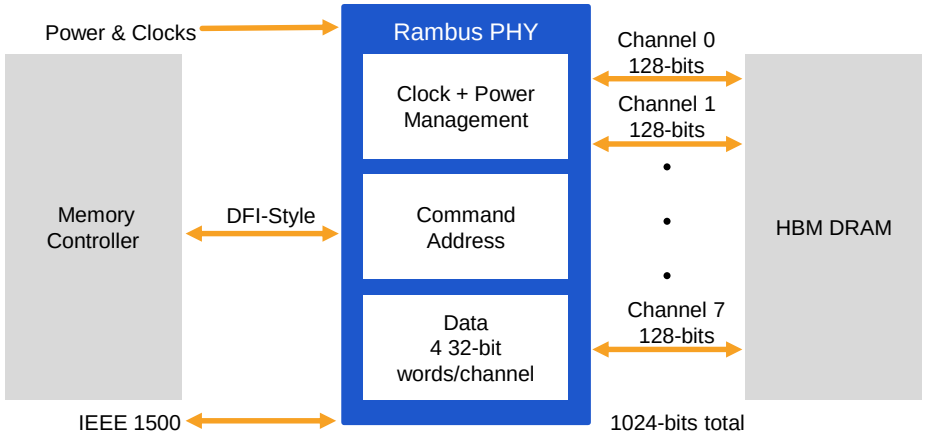
Rambus HBM PHY Overview

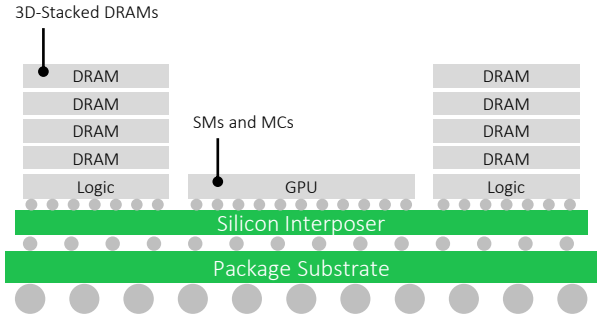
Advantages:

- Production experience: 2yrs
- Hardened Timing closed PHY
- System Design Support: Interposer and Package
- Lab Station development environment: Bring-up support

Features:

- 410GB/s bandwidth
- Max speed bins: 2, 2.4, 2.8, 3.2Gbps
- DRAMs: Stack height of 2, 4, 8
- Channels: 8 x 128bits
- ASIC Interface: DFI style
- Lane repair
- IEEE 1500 test support
- PHY independent mode





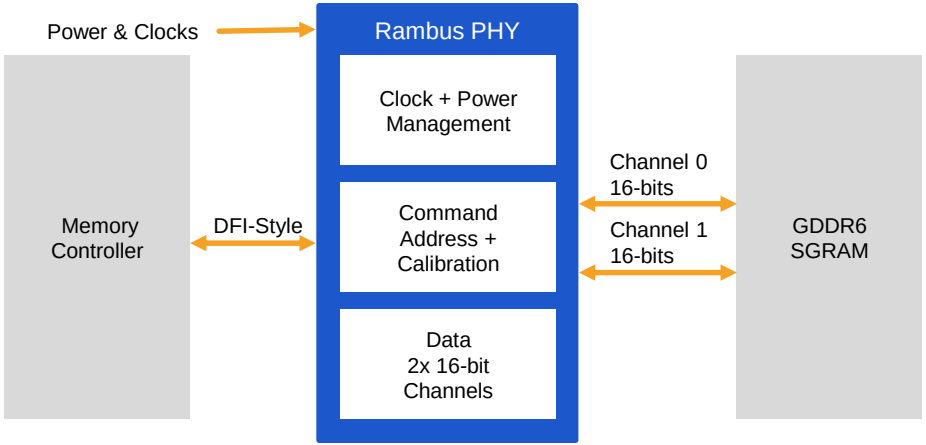
Rambus GDDR6 PHY Overview

Advantages:

- GDDR6 working silicon in lab
- System design support: PCB and package design support
- SI/PI expertise
- Complete timing closed macro

Features:

- 512Gbit/s bandwidth
- Speed Bins: 12, 14, 16Gbps
- Supported DRAM: 8, 12, 16Gbit
- ASIC Interface: DFI style
- Clam Shell mode supported
- All training and calibration modes support
- PHY independent mode



High-Speed Memory Development Hardware

Summary

- Exponential data growth is driving the need for higher speed data links and increased memory bandwidth
- Memory bandwidth a critical resource for emerging applications
- HBM: Extremely high bandwidth and power efficiency
- GDDR: Good tradeoff between bandwidth, capacity, power efficiency, cost, reliability, design complexity
- Rambus is more than a PHY supplier
  - SI/PI expertise for 2.5D and 3D systems
  - Advanced SI/PI tools developed over last 20 years

Thank you

Rambus

Data · Faster · Safer